In the Claims:

Claim 1 (original) Apparatus for the design of logic circuits, comprising:

a. a computer, and

b. software stored on the computer for

b1. representing multilevel logic schema in vector form; and for

b2. simplifying multilevel logic schema into a simplified form by exploiting symmetries in the logical schema.

Claim 2 (original) The apparatus of claim 1 in which simplifying multilevel logic schema comprises eliminating opposing couples.

Claim 3 (original) A method of reducing multilevel logic to simpler form comprising the steps of:

a. representing the logic in vector form; and

b. removing redundancy by eliminating opposing couples.

Claim 4 (original) The method of claim 3 further comprising the step of:

c. sliding symmetrical portions of the logic attached to opposing couples onto a point common to the opposing couples.

Claim 5 (original) A system for the design or manufacturing of logical circuits, comprising:

a. a plurality of computers connected to a network;

b. at least one of said computers having software stored thereof for

b1. representing multilevel logic schema in vector form; and for

b2. simplifying multilevel logic schema into a simplified form by exploiting symmetries in a logical schema.

Claim 6 (original) The system of claim 5 in which a computer having said software communicates logical schema to one or more other computing devices.

Claim 7 (original) The system of claim 5 in which the software eliminates opposing couples in simplifying multilevel logic.

Claim 8 (original) A computer program product, comprising:

a. a computer readable storage medium; and

b. at least one computer program stored on said storage medium, said at least one computer program comprising instructions for:

b1. representing multilevel logic schema in vector form; and for

b2. simplifying multilevel logic schema into a simplified form by exploiting symmetries in the logical schema.

Claim 9 (original) A computer program product, comprising:

a. a computer readable storage medium; and

b. at least one computer program stored on said storage medium, said at least one computer program comprising instructions for:

b1. representing the logic in vector form; and

b2. removing redundancy by eliminating opposing couples.

Claim 10 (original) A method of manufacturing integrated circuits comprising the steps of:

a. representing at least a portion of the logic circuits to be incorporated into the integrated circuit in vector form; and

b. simplifying the logic by removing redundancy by eliminating opposing couples.

Claim 11 (original) A method of manufacturing integrated circuits comprising the steps of:

a. representing at least a portion of the logic circuits to be incorporated into the integrated circuit in vector form; and

b. simplifying the logic by removing redundancy by exploiting symmetries in the logical schema.

Claim 12 (original) A method of reducing multilevel logic to simpler form comprising the steps of:

a. representing the logic in vector form;

b. identifying opposing couples having at least symmetrical logic comprising some similarities in logical expression that connects to them;

c. removing redundancy by eliminating an opposing couples and sliding the symmetrical logic attached to opposing couples onto a point common to the opposing couples.